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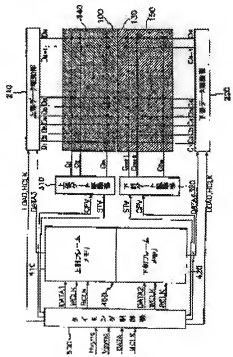
(54) LIQUID CRYSTAL DISPLAY DEVICE AND ITS DRIVING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent brightness non-uniformity at the interfacial part of the two panels by reversing the scanning direction of the upper panel with respect to the scanning direction of the lower panel when dividing the liquid crystal display panel into two panels of the upper panel and the lower panel and applying a scanning signal to a gate line.

SOLUTION: The display panel is constituted of an upper panel 140 and a lower panel 150. An upper and a lower gate driving parts 310, 320 are connected to an upper and a lower gate line blocks respectively, and apply a gate-on voltage one by one to the gate line of the gate line block along a reverse scanning direction. For example, when the upper gate driving part 310 drives a gate-on voltage in the direction from the first gate line G1 of the upper gate line block to the m-th gate line Gm (that is, direction from the top to the bottom), the lower gate driving part



320 drives a gate-on voltage in the direction from the last gate line G2m of the lower gate line block to the first gate line Gm+1 (that is, direction from the bottom to the top).

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a drawing in which the liquid crystal display using a dual-scan method is shown.
[Drawing 2]It is a drawing in which the drive method **** signal wave form of the conventional liquid crystal display is shown.
[Drawing 3]It is a schematic diagram showing the liquid crystal display by the desirable example of this invention.
[Drawing 4]It is a drawing in which the timing of the data which reads with a writing clock signal, and is outputted and inputted by each frame synchronizing with a clock signal is shown.

[Drawing 5]It is a circuit diagram showing the polarity of a liquid crystal display and the scanning direction which are shown in drawing 3 by the 1st example of this invention.
[Drawing 6]It is a drawing in which the waveform of the signal by the 1st example of this invention is shown.
[Drawing 7]It is a circuit diagram showing the polarity of the liquid crystal display shown in drawing 3 by the 2nd example of this invention, and a scanning direction.
[Drawing 8]It is a drawing in which the waveform of the signal by the 2nd example of this invention is shown.
[Drawing 9]It is a circuit diagram showing the polarity of the liquid crystal display shown in drawing 3 by the 3rd example of **********, and the 4th example, and a scanning direction.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a liquid crystal display and a drive method for the same. This invention relates to a liquid crystal display which has a screen which it is divided into two portions and driven, respectively, and a drive method for the same in more detail.
[0002]
[Description of the Prior Art]As for the display device, a weight saving and by thin-type-izing, a weight saving and thin type-ization are demanded for a personal computer or television. Therefore, it is increasing [******] instead of a monotonous display like LCD being a cathode-ray tube (CRT). In order to acquire a desired picture signal, LCD impresses an electric field (electricfield) to the liquid crystal material which has the anisotropy dielectric constant poured in between two substrates, and adjusts the quantity of the light penetrated through a substrate with field strength. LCD is one of the portable monotonous displays most generally used.
[0003]TFT-LCD which adopted the thin film transistor (thin film transistor;TFT) as a switching element especially is used widely. Said LCD contains the gate line of a large number which transmit a scanning signal. The data line of a large number which intersect said gate line transmits image data. The pixel of a large number formed in the field formed by said gate line and the data line is mutually connected through a gate line, the data line, and a switching element.
[0004]Hereafter, how to impress image data to each pixel in such LCD is explained. When the scanning signal (or gate ON signal) which makes a gate one is impressed to a gate line one by one, the switching element connected with said gate line is turned on one by one. The picture signal (namely, gradation voltage (data vol-tage)) impressed to the pixel row corresponding to said gate line is simultaneously impressed to each data line. The picture signal impressed to

said data line is impressed to each pixel through the switching element by which turn-on is carried out after that. At this time, by impressing a gate ON signal to all the gate lines one by one between 1 frame periods, a picture signal is impressed to all the pixel rows, and the picture of one frame is displayed.

[0005]The gate line of many [LCD / which was developed these days / high resolution] is required. However, since the time concerning scanning one frame is restricted to 1 / 60 seconds, the time interval (time interval) of the gate ON signal impressed to each gate line becomes short. For this reason, it is difficult to impress sufficient picture signal (gradation voltage) for said image line through a switching element, and it reduces image quality.

[0006]Therefore, in order to secure gate ON time sufficient these days, the method which divides a display screen into two portions (upper part and lower part), and drives a liquid crystal display is proposed. Such a drive system is called 'dual-scan method'. Drawing 1 shows the liquid crystal display which adopted the dual-scan method. The liquid crystal display which uses a dual-scan method consists of the liquid crystal display panel 10, the top data actuator 21, the lower data actuator 22, the upper gate actuator 31, and the lower gate actuator 32 as shown in drawing 1.

[0007]The liquid crystal display panel 10 contains many gate lines (G1, G2, ..., Gm, Gm+1, ..., G2m) for transmitting a gate ON signal, and much data lines (D1, D2, ..., Dn, C1, C2, ..., Cn) for transmitting gradation voltage (namely, picture signal). The field formed by intersection with a gate line and the data line forms a pixel. Each pixel contains the picture element electrode 14 connected with the drain electrode of the thin film transistor 12 and the thin film transistor 12 in which a gate electrode is connected with a gate line, and a source electrode is connected with the data line, and the common electrode (not shown) in which common voltage is impressed. The gate line of said large number is divided into the upper part and the lower gate line block which consist of m gate lines (G1, G2, .. Gm) and (Gm+1, ..., G2m), respectively. the data line (D1, D2, and ....) connected with the pixel corresponding to the gate line (G1, G2, .. Gm) of an upper gate line block Dn) is separated from the data line (C1, C2, ..., Cn) connected with the pixel corresponding to the gate line (Gm+1, ..., G2m) of a lower gate line block. For example, the top pixel of the 1st row is connected with the data line D1, and the lower pixel of the 1st row is connected with the data line C1.

[0008]The upper part and the lower gate actuators 31 and 32 which are connected with the upper part and a lower gate line block, respectively impress gate ON state voltage to the gate line of the upper part and a lower gate line block one by one, respectively. At this time, gate ON state voltage is most impressed to a gate line in order of the last gate line from the gate line of eyes. The upper part and the lower data actuators 21 and 22 which are formed in the upper part and the lower part of a liquid crystal display panel, respectively impress gradation voltage to the top data line (D1, D2, ..., Dn) and the lower data line (C1, C2, ..., Cn),

respectively.

[0009]Hereafter, operation of said liquid crystal display is explained. A gate ON signal is impressed to the gate line which begins from the 1st gate line and follows the thin film transistor 12 further from the gate line of the upper part and a lower gate line block one by one at it. It can come, simultaneously gradation voltage (namely, picture signal) is impressed to the upper part and the lower data line. By said gate ON signal, turn-on of the thin film transistor 12 is carried out, and the gradation voltage impressed to the data line is impressed to a picture element electrode through the thin film transistor 12 by which turn-on was carried out. The electric field produced according to the difference of picture element voltage (namely, voltage impressed to the picture element electrode) and the common voltage of a common electrode is impressed to liquid crystal material. Since the arrangement of liquid crystal material changes according to field strength (field strength is changed according to the strength of gradation voltage), the quantity of the light which penetrates liquid crystal material comes to change. Therefore, a desired picture is displayed on a liquid crystal display.

[0010]Since said gate ON signal is simultaneously impressed to the gate line of said upper part and a lower gate line block, it has the strong point in which the liquid crystal display of the above-mentioned dual-scan method has gate ON time twice as long as the conventional single scan liquid crystal display. If the electric field of a uniform direction is impressed succeeding liquid crystal material, liquid crystal material will deteriorate. Therefore, when gradation voltage drives, the polarity of gradation voltage becomes positive and negative by turns. Such a drive system is called inversion driving method.

[0011]There are a frame-inversion-driving method which reverses polarity per frame, a line-inversion-driving method which reverses polarity per line, and a dot inversion driving system which makes a pixel unit reverse polarity in the type of an inversion driving method. Said line inversion and a dot inversion driving system are most generally used. However, when applied to the liquid crystal display of the conventional dual-scan method, a problem which is explained below generates a line-inversion-driving method or a dot inversion driving system.

[0012]The pixel of the liquid crystal display of drawing 1 assumes that it drives with a dot inversion driving system as shown by right (+) and negative (-). A sun (+) pole shows here that the polarity of the picture element voltage to common voltage is positive, and a shade (-) pole shows that the polarity of the picture element voltage to common voltage is negative. The waveform of the voltage impressed to the picture element electrode electrically connected with the waveform of the voltage impressed to the picture element electrode electrically connected with the gate line Gm and the data line D1 of said upper gate line block, gate line Gm+1 of said lower gate line block, and the data line C1 is shown in drawing 2.

[0013]In ideal conditions, the voltage Vpu lower than the common voltage Vcom is uniformly impressed to the picture element electrode of the 1st pixel row connected with the gate line

Gm of the last of an upper gate line block between 1 frame periods as shown in drawing 2. However, in a actual liquid crystal display, in order that parasitism capacitance may generate between a picture element electrode and the data line, the picture element voltage impressed to a actual picture element electrode is influenced by the voltage impressed to the data line. That is, since gradation voltage Vd1 by which the polarity about the common voltage Vcom is repeated periodically is impressed to the 1st data line D1 as shown in drawing 2 (a), the actual voltage Va impressed to a picture element electrode comes to have a waveform like drawing 2 (b). For the facilities of explanation, it is assumed that gradation voltage is symmetrical about the common voltage Vcom.

[0014]When the gradation voltage Vd which the picture element voltage Vpu which has negative polarity is impressed, and has positive polarity in the data line is impressed in more detail as shown in drawing 2 (a) and (b), The actual picture element voltages Va differ in the ideal picture element voltage Vpu, and only deltaV is pulled by the influence of parasitism capacitance in the direction of common voltage. When the gradation voltage which has negative polarity this and reversely is impressed to the data line, the actual picture element voltage Va is pulled in the direction of the common voltage and the contrary of only deltaV.

[0015]When ideal, the constant voltage Vpd higher than the common voltage Vcom is impressed to the picture element electrode of the 1st pixel row connected with 1st gate line Gm+1 of a lower gate line block between 1 frame periods, as shown in drawing 2 (c). The gradation voltage which has the polarity of the gradation voltage impressed to the data line D1 and the same polarity is impressed to the 1st data line C1. It is because this has the same polarity of the picture element voltage which the scan began from each 1st gate line of an upper gate line block and a lower gate line block, and was connected with the 1st gate line of the upper gate line block and the lower gate line block.

[0016]Therefore, the voltage actually impressed to a picture element electrode has a waveform like drawing 2 (d) under the influence of parasitism capacitance. Namely, when the gradation voltage which the picture element voltage Vpd which has positive polarity is impressed, and has positive polarity is impressed to the data line as shown in drawing 2 (c) and (d), Unlike the ideal picture element voltage Vpu, the actual picture element voltage Vb is pulled by the influence of parasitism capacitance in the direction of the common voltage and the contrary of only deltaV. When the gradation voltage which has negative polarity is impressed to the data line, the actual picture element voltage Vb is pulled only deltaV in the direction of common voltage.

[0017]As a result, since the voltage impressed to the data line at the pixel of two pixel rows of an interface affects a counter direction, the actual difference of the voltage and common voltage which are impressed to a pixel becomes the portion shown in drawing 2 (b) and (d) with the slash. Therefore, the difference of the quantity of the light which penetrates liquid

crystal material in the pixel of the boundary part of an upper block and a lower block assembly becomes large, and luminosity unevenness occurs in a boundary part by this. After all, the line which is not desirable appears in the boundary part of an upper block and a lower block assembly.

The purpose of outline this invention of an invention is to provide a liquid crystal display which divides a display screen into two panels, drives it, and prevents the luminosity heterogeneous phenomena of the boundary part of two panels, and a drive method for the same.

[0018]In order to attain such a purpose, the liquid crystal display panel of this invention is divided into two panels, an upper panel and a lower panel. When impressing a scanning signal to a gate line, since the scanning direction of an upper panel is opposite to the scanning direction of a lower panel, the unevenness of the luminosity of the boundary part of a panel is prevented. The 1st gate line block whose liquid crystal display by this invention contains the 1st gate line of a large number which transmit a scanning signal, The 2nd gate line block containing the 2nd gate line of a large number which transmit a scanning signal, The 1st data line of a large number which transmit a picture signal and intersect the 1st gate line of said 1st gate line block, The 2nd data line of a large number which are separated from said 1st data line and intersect the 2nd gate line of said 2nd gate line block, It consists of a pixel of a large number which have a switching element which is formed in the field surrounded by said gate line and the data line, is arranged by the matrix form, and is connected with said gate line and the data line, and the scanning direction of said 1st gate line is opposite to the scanning direction of said 2nd gate line.

[0019]The number of said 1st gate lines is the same as the number of said 2nd gate lines. Said 1st gate line and the 2nd gate line are scanned simultaneously. The 1st gate line block with which other features of the liquid crystal display of this invention have many 1st gate line, The 2nd gate line block which is formed under said 1st gate line block, and has many 2nd gate line, The 1st data line of a large number which intersect the 1st gate line of said 1st gate line block, and are separated, The 2nd data line of a large number which intersect the 2nd gate line of said 2nd gate line block, and are separated, The liquid crystal display panel containing the pixel of a large number arranged by the matrix form which has a switching element which is formed of the field surrounded by said gate line and the data line, and is connected with said gate line and the data line, and a common electrode in which common voltage is impressed is included. The 1st data actuator which impresses the gradation voltage in which a liquid crystal display has a picture signal to said 1st data line, The 2nd data actuator which impresses the gradation voltage which has a picture signal to said 2nd data line, The 1st gate actuator which impresses a scanning signal to the gate line of said 1st gate line block, The 2nd gate actuator which impresses a scanning signal to the gate line of said 2nd gate line block in the scanning direction and counter direction of said 1st gate actuator, The 1st frame memory that writes

down in response to the input of a picture signal from the exterior, records synchronizing with a clock signal, and outputs said picture signal to said 1st data actuator synchronizing with a reading clock signal, The 2nd frame memory that writes down in response to the input of a picture signal from the exterior, records synchronizing with a clock signal, and outputs said picture signal to said 2nd data actuator synchronizing with a reading clock signal is included.
[0020]The number of said 1st gate lines is the same as the number of said 2nd gate lines. Said 1st gate actuator and the 2nd gate actuator are scanned simultaneously. The polarity to said common voltage of the gradation voltage impressed to the pixel connected with the gate line with which said 1st gate line block adjoins is mutually opposite, and the polarity to said common voltage of the gradation voltage impressed to the pixel connected with the gate line with which said 2nd gate line block adjoins is mutually opposite. Said 1st gate actuator impresses a scanning signal in the direction of the gate line of eyes one by one most from the gate line of the last of said 1st gate line block at a gate line, Said 2nd gate actuator impresses a scanning signal in the direction of the last gate line one by one from the first gate line of said 2nd gate line block at a gate line. Said 1st frame memory outputs the picture signal impressed to said 1st data line, and the picture signal recorded on an opposite order to said 1st data actuator, Said 2nd frame memory outputs the picture signal impressed to said 2nd data line, and the picture signal recorded on the same order to said 2nd data actuator.
[0021]The polarity of said common voltage to the gradation voltage impressed to the pixel connected with the gate line of the last of said 1st gate line block by the same pixel row is opposite to the polarity of the common voltage to the gradation voltage impressed to the pixel of said 2nd gate line block most connected with the gate line of eyes. The polarity of the common voltage to the gradation voltage impressed to the pixel connected with the gate line of the last of said 1st gate line block is the same as the polarity of the common voltage to the gradation voltage impressed to the pixel of said 2nd gate line block most connected with the gate line of eyes. Said 1st gate actuator impresses a scanning signal in the direction of the last gate line one by one from the first gate line of said 1st gate line block at said gate line, Said 2nd gate actuator impresses a scanning signal in the direction of the gate line of eyes one by one most from the gate line of the last of the 2nd gate line block at said gate line. Said 1st frame memory outputs the picture signal recorded on the same order as an order that a picture signal is impressed to said 1st data line to the 1st data actuator, Said 2nd frame memory outputs the picture signal recorded on an order opposite to an order that a picture signal is impressed to said 2nd data line to the 2nd data actuator. The polarity of the common voltage to the gradation voltage impressed to the pixel connected with the gate line of the last of said 1st gate line block by the same pixel row is opposite to the polarity of the common voltage to the gradation voltage impressed to the pixel of said 2nd gate line block most connected with the gate line of eyes. The polarity of the common voltage to the gradation voltage impressed to the

pixel connected with the gate line of the last of said 1st gate line block by the same pixel row is the same as the polarity of the common voltage to the gradation voltage impressed to the pixel of said 2nd gate line block most connected with the gate line of eyes.

[0022]As a feature of others of the drive method of the liquid crystal display of this invention, The 1st gate line block which has the 1st gate line of a large number formed horizontally, The 2nd gate line block which is formed under said 1st gate line block, and has many 2nd gate line, The 1st data line of a large number which intersect the 1st gate line of said 1st gate line block, and are separated, The stage of being a drive method of the liquid crystal display which intersects the 2nd gate line of said 2nd gate line block, and contains the 2nd data line of a large number separated, and impressing a scanning signal to the 1st gate line of said 1st gate line block one by one, The stage of impressing a scanning signal to the 2nd gate line of said 2nd gate line block in a scanning direction opposite to said 1st gate line one by one, The stage of impressing gradation voltage to the pixel connected with said gate line which impresses the gradation voltage which includes a picture signal in said 1st and 2nd data lines, and with which said scanning signal is impressed is included.

[0023]Said scanning signal is most impressed in the direction of the gate line of eyes one by one from the last gate line at said 1st gate line block, and is most impressed in the direction of the last gate line one by one from the gate line of eyes at said 2nd gate line block. The stage where such a method records the picture signal impressed to said 1st data line of the picture signals inputted from the outside on the 1st frame memory, The stage which records the picture signal impressed to said 2nd data line of the picture signals inputted from the outside on the 2nd frame memory, The stage which outputs said picture signal to said 1st data line at an order opposite to an order that a picture signal is recorded on said 1st frame memory, and an order that a picture signal is recorded by said 2nd frame memory and the stage which outputs said picture signal to said 2nd data line at an opposite order are included further. Said scanning signal is most impressed in the direction of the last gate line one by one from the gate line of eyes at said 1st gate line block, and is most impressed in the direction of the gate line of eyes one by one from the last gate line at said 2nd gate line block. The stage which records the picture signal impressed to said 1st data line of the picture signals inputted from the outside on the 1st frame memory, The stage which records the picture signal impressed to said 2nd data line of the picture signals inputted from the outside on the 2nd frame memory, The stage which outputs said picture signal to said 1st data line at an order opposite to an order that a picture signal is recorded on said 1st frame memory, and an order that a picture signal is recorded by said 2nd frame memory and the stage which outputs said picture signal to said 2nd data line at an opposite order are included further.

[0024]

[Embodiment of the Invention]Based on the drawing of the most desirable gestalt predicted in

connection with an artificer inventing, below only the desirable example of this invention is shown and it is explained to it. Various modification is possible for this invention within the limits of an invention. Therefore, a drawing and an embodiment are only examples and do not limit an invention.

[0025]Drawing 3 shows the liquid crystal display by the desirable example of this invention. A liquid crystal display The liquid crystal display panel 100 and the top data actuator 210, It becomes the lower data actuator 220, the upper gate actuator 310, the lower gate actuator 320, and the frame memory unit 400 containing the top frame memory 410 and the lower frame memory 420 from the timing-control machine 500.

[0026]The liquid crystal display panel 100 contains the 2m piece gate line (G1, G2, ..., Gm+1, ..., G2m) for transmitting a gate ON signal, and the data line (D1, D2, ..., Dm, and C1, C2, ..., Cn) for transmitting the gradation voltage which displays a picture signal. The field surrounded by a gate line and the data line forms a pixel, and each pixel, The thin film transistor 110, the gate line connected with a gate electrode, the data line connected with a source electrode, the picture element electrode 120 connected with the drain electrode of said thin film transistor 110, and the common electrode (not shown) in which the seal of approval of the common voltage is carried out are included as shown in drawing 5. The 2m piece gate line is divided into the upper gate line block containing m gate lines (G1, G2, ..., Gm) and the lower gate line block which has m gate lines (Gm+1, Gm+2, ..., G2m). the top data line (D1, D2, and ....) connected with the pixel corresponding to the gate line (G1, G2, Gm) of an upper gate line block Dn) is separated from the lower data line (C1, C2, Cn) connected with the pixel corresponding to the gate line (Gm+1, Gm+2, G2m) of a lower gate line block. That is, the liquid crystal display panel by the example of this invention consists of the upper panel 140 and the lower panel 150. Said upper panel 140 contains an upper gate line block and the top data line (D1, D2, ..., Dn), and the lower panel 150 contains a lower gate line block and the lower data line (C1, C2, ..., Cn).

[0027]The upper part and the lower gate actuators 310 and 320 are connected with the upper part and a lower gate line block, respectively, and impress gate ON state voltage to the gate line of a gate line block in an opposite scanning direction one by one. An upper gate line block most For example, the direction of the gate line G1 of eyes to the m-th gate line Gm. [the upper gate actuator 310] When driving gate ON state voltage in (namely, the direction of a top to the bottom), the lower gate actuator 320 drives gate ON state voltage most in the direction of gate line Gm+1 of eyes (namely, the direction of the bottom to a top) from the gate line G2m of the last of a lower gate line block. As mentioned above, when the upper gate actuator 310 impresses gate ON state voltage in the direction of [upper] one by one from the bottom at a gate line, as for the lower gate actuator 320, gate ON state voltage is impressed in the direction of [lower] from a top at a gate line.

[0028]The top data actuator 210 and the lower data actuator 220 are formed in the upper part and the lower part of a liquid crystal display panel, and are connected with the top frame memory 410 and the lower frame memory 420, respectively. These impress the gradation voltage which displays a picture signal on the top data line (D1, D2, ..., Dn) and the lower data line (C1, C2, ..., Cn), respectively.

[0029]The timing-control machine 500 Image data signal DATA, the main clocks MCLK. In response to the input of Horizontal Synchronizing signal Hsync and Vertical Synchronizing signal Vsync, a timing signal is impressed to the frame memory unit 400, the upper gate actuator 310, the lower gate actuator 320, the top data actuator 210, and the lower data actuator 220. The top frame memory 410 and the lower frame memory 420, Read with writing clock signal WCLK and it synchronizes with clock signal RCLK (the frequency of this is 1/2 of writing clock signal WCLK impressed from the timing-control machine 500), The writing and reading of an image data signal which are impressed to the top data actuator 210 and the lower data actuator 220 are performed.

[0030]Hereafter, operation of the liquid crystal display by the 1st example of this invention is explained. Drawing 4 (a) and (b) is a data timing diagram which reads with writing clock signal WCLK, and data is inputted into a frame memory and outputted to it synchronizing with clock signal RCLK (RCLK=WCLK/2). Image data signal DATA, the main clocks MCLK, Vertical Synchronizing signal Vsync (namely, frame alignment signal), and Horizontal Synchronizing signal Hsync (namely, synchronized signal of a horizontal line or a scan line) are inputted into the timing-control machine 500 from the exterior.

[0031]A frame memory records data synchronizing with writing clock signal WCLK impressed from the timing-control machine 500 as shown in drawing 4 (a). That is, data is recorded on an order which begins from the image data d1 most impressed to the pixel row of eyes by the top frame memory 410 synchronizing with writing clock signal WCLK. At this time, the image data (d1, d2, ..., dm) most impressed to the m-th pixel row (namely, pixel row corresponding to the gate line of an upper gate line block) from the pixel row of eyes is recorded on the top frame memory 410. In contrast, the image data (dm+2, ..., d2m) which starts in image data dm+1 impressed to the pixel row most corresponding to gate line Gm+1 of eyes of a lower gate line block is recorded on the lower frame memory 420 in order synchronizing with writing clock signal WCLK.

[0032]If all the image data impressed to each pixel row is recorded on the top frame memory 410 and the lower frame memory 420, the image data in sync with reading clock signal RCLK will be transmitted to the top data actuator 210 or the lower data actuator 220 as shown in drawing 4 (b). According to the 1st example of this invention at this time, the image data for the top data actuator 210 is transmitted to an order (namely, dm and dm-1, dm-2, ..., d2, d1) opposite to an order recorded on the top frame memory 410 at the top data actuator 210. The

image data for the lower data actuator 220 is transmitted to the same order as an order recorded on the lower frame memory 420 at the lower data actuator 220. Therefore, according to this invention, as a frame memory, the memory by which addressing may be carried out to an order opposite to an order recorded must be used.

[0033]If the image data in sync with clock signal HCLK is transmitted to the top data actuator 210 and the lower data actuator 220, Image data is changed into corresponding gradation voltage, and is impressed to each line of the top data line D1, D2, ..., Dn and the lower data line C1, C2, ..., Cn by load signal LOAD outputted from the timing-control machine 500.

[0034]The upper gate actuator 310 and the lower gate actuator 320 synchronize with the start signal STV and the gate clock CPV which are outputted from the timing-control machine 500, and to the gate line of an upper gate line block Gate ON state voltage. (Namely, a scanning signal) is impressed and gate ON state voltage is simultaneously impressed also to the gate line of a lower gate line block. According to the 1st example of this invention at this time, the upper gate actuator 310 impresses gate ON state voltage in the direction of the first gate line G1 of an upper gate line block (namely, the direction of the bottom to a top) one by one from the gate line Gm of the last of an upper gate line block. The lower gate actuator 320 impresses gate ON state voltage in the gate line [of the last of a lower gate line block / G2m] direction (namely, the direction of a top to the bottom) one by one from first gate line Gm+1 of a lower gate line block.

[0035]Turn-on of the thin film transistor connected with the gate line with which gate ON state voltage was impressed is carried out, the gradation voltage impressed to the data line in connection with this is transmitted to a picture element electrode through the thin film transistor by which turn-on was carried out, and a desired picture is displayed. A striped pattern can be prevented from generating the example of such this invention in the center of a screen, when driving dual-scan LCD using dot inversion or a line inversion method.

[0036]Drawing 5 is a drawing in which the scanning direction of the upper gate actuator 310 by the 1st example of this invention and the lower gate actuator 320 and polarity are shown. Drawing 6 (a), (b), (c), and (d) are drawings in which the waveform of the signal by the 1st example of this invention is shown. (+) shows that the polarity of the picture element voltage to common voltage is positive, and (-) shows that the polarity of the picture element voltage to common voltage is negative as shown in drawing 5.

[0037]Hereafter, two pixels which the 1st pixel row adjoins are explained as an example. When ideal, the voltage Vpu lower than the common voltage Vcom is uniformly impressed to the picture element electrode of the 1st pixel row connected with the gate line Gn of the last of an upper gate line block between 1 frame periods, as shown in drawing 6 (a). However, the actual picture element voltage impressed to a picture element electrode is influenced by the voltage impressed to the data line for the parasitism capacitance generated between a picture element

electrode and the data line. That is, since the gradation voltage by which the polarity to common voltage is repeated periodically is most impressed to the top data line D1 of eyes, the actual voltage Va impressed to a picture element electrode becomes like drawing 6 (b). Negative and positive are continuously repeated as the gradation voltage which a gate line is scanned in the direction of [upper] from the bottom at this time, and is impressed to the data line D1 since the polarity of the picture element electrode corresponding to the gate line Gm of the last of the 1st pixel row is negative is shown in drawing 6 (a).

[0038]In more detail, the picture element voltage Vpu which has the polarity of shade (-) is impressed as shown in drawing 6 (a) and (b), When the gradation voltage which has the polarity of shade (-) is impressed to the data line, the actual picture element voltage Va is pulled by the counter direction of common voltage only deltaV compared with the ideal picture element voltage Vpu under the influence of the parasitism capacitance Cp. In contrast, when the gradation voltage which has the polarity of the sun (+) is impressed to the data line, the actual picture element voltage Va is pulled in the common voltage direction only deltaV.

[0039]When ideal, the voltage Vpd higher than the common voltage Vcom is uniformly impressed to the picture element electrode of the 1st pixel row of a lower gate line block most connected with gate line Gm+1 of eyes between 1 frame periods, as shown in drawing 6 (c). The gradation voltage which has different polarity from the gradation voltage impressed to the data line D1 is most impressed to the lower data line C1 of eyes. An upper gate line block is scanned in the direction of [upper] from the bottom as this is shown in drawing 5, It is because the picture element voltage Vpu which a lower gate line block is scanned in the direction of [lower] from a top, and is connected with the gate line Gm of the last of an upper gate line block differs from the picture element voltage of a lower gate line block most connected with gate line Gm+1 of eyes. Therefore, the actual voltage impressed to a picture element electrode under the influence of the parasitism capacitance Cp has a waveform as shown in drawing 6 (d). Namely, when the gradation voltage which the picture element voltage Vpd which has the polarity of (+) is impressed, and has the polarity of (+) is supplied to the data line namely, as shown in drawing 6 (c) and (d). The actual picture element voltage Vb is pulled by the counter direction of common voltage only deltaV under the influence of the parasitism capacitance Cp compared with the ideal picture element voltage Vpd. When the gradation voltage which has the polarity of (-) is impressed to the data line, the actual picture element voltage Vb is pulled in the common voltage direction only deltaV.

[0040]As mentioned above, in order that the voltage impressed to the data line may affect the pixel of two pixel rows which exist in an interface in a uniform direction according to the 1st example of this invention, the difference of the voltage and common voltage which are impressed to a actual pixel is as being shown to drawing 6 (b) and (d) by the slash. Therefore, since the difference of the quantity of the light which penetrates the liquid crystal material in the

pixel of a boundary part is small, the luminosity in a boundary part almost becomes homogeneity. Therefore, the striped pattern generated in the boundary part of an upper panel and a bottom panel in the conventional dual-scan LCD drive system does not occur.

[0041]Hereafter, operation of the liquid crystal display by the 2nd example of this invention is explained. Drawing 7 is a circuit diagram showing the scanning direction of the upper part of the liquid crystal display by the 2nd example of this invention, and a lower gate actuator, and polarity. Drawing 8 shows the waveform of various kinds of signals by the 2nd example of this invention. The polarity of two pixels which a boundary part adjoins is mutually the same, and the polarity of the pixel of others of a boundary part is reversed as shown in drawing 7. Hereafter, two pixels which the 1st pixel row adjoins are explained as an example.

[0042]When ideal, the picture element voltage Vpu higher than the common voltage Vcom is uniformly impressed to the picture element electrode of the 1st pixel row connected with the gate line Gm of the last of an upper gate line block between 1 frame periods, as shown in drawing 8 (a). However, the actual picture element voltage impressed to a picture element electrode is influenced by the voltage impressed to the data line for the parasitism capacitance Cp produced between a picture element electrode and the data line.

[0043]That is, since the gradation voltage by which the polarity to common voltage is repeated periodically is impressed to the top data line D1 which are eyes most, the voltage Va impressed to a actual picture element electrode comes to be shown in drawing 8 (b). At this time, a gate line is scanned in the direction of [upper] from the bottom, and since the polarity of the picture element electrode corresponding to the gate line Gm of the last of the 1st pixel row is positive, the gradation voltage impressed to the data line D1 is reversed in order of positive, negative, positive, negative, and ... as shown in drawing 8 (a).

[0044]In more detail, the picture element voltage Vpu which has positive polarity is impressed as shown in drawing 8 (a) and (b), When the gradation voltage which has positive polarity is impressed to the data line, as compared with the picture element voltage Vpu with the actual ideal picture element voltage Va, only deltaV is pulled by the influence of parasitism capacitance in the counter direction of common voltage. On the other hand, if the gradation voltage which has negative polarity is impressed to the data line, said picture element voltage Va will be pulled in the common voltage direction only deltaV.

[0045]When ideal, the picture element voltage Vpd higher than the common voltage Vcom is impressed to the picture element electrode of the 1st pixel row of a lower gate line block most connected with gate line Gm+1 of eyes between 1 frame periods, as shown in drawing 8 (c). The gradation voltage impressed to the data line D1 and the gradation voltage which has the same polarity are impressed to the lower data line C1 which are eyes most. An upper gate line block is scanned in the direction of [upper] from the bottom as this is shown in drawing 7, It is because the polarity of the picture element voltage which a lower gate line block is scanned in

the direction of [lower] from a top, and is connected with the gate line Gm of the last of an upper gate line block is the same as the polarity of the picture element voltage connected with gate line Gm+1 of a lower gate line block which is eyes most. Therefore, the voltage impressed to a actual picture element electrode has a waveform like drawing 8 (d).

[0046]In order that the voltage impressed to the data line may affect the pixel of two pixel rows in an interface in a uniform direction according to the 2nd example of this invention as shown in drawing 8, a slash came to have shown the difference of the actual voltage and common voltage which are impressed to a pixel to drawing 8 (b) and (d). Therefore, since the difference of the quantity of the light which penetrates the liquid crystal material in the pixel of a boundary part is small, the luminosity of a boundary part almost becomes homogeneity. Therefore, the striped pattern generated in the boundary part of the conventional upper panel and a bottom panel does not appear.

[0047]In the example of above-mentioned this invention, the gate line connected with the upper gate actuator is scanned in the direction of [upper] from the bottom, and the gate line connected with the lower gate actuator is scanned in the direction of [lower] from a top. However, the gate line connected with the upper gate actuator is scanned from a top to the bottom, and also when scanned in the direction of [upper] from the bottom, the gate line connected with the lower gate actuator is included as the drive method of the liquid crystal display by this invention is shown in drawing 9 (a) and (b).

[0048]Hereafter, based on drawing 9 (a) and (b), the drive method of the liquid crystal display by the 3rd and 4th examples of this invention is explained. A gate line is scanned in the direction of the boundary part of a panel from the end of the upper part and a lower liquid crystal display panel. That is, according to the 3rd example of this invention, a gate line is scanned in the direction of the boundary part of a panel from the end of the upper part and a lower liquid crystal display panel, and the picture element voltage which has mutually different polarity is impressed to two pixels which adjoined the boundary part as shown in drawing 9 (a). According to the 4th example of this invention, a gate line is scanned in the direction of the boundary part of a panel from the end of the upper part and a lower liquid crystal display panel, and the picture element voltage which has the same polarity is impressed to two pixels which adjoined the boundary part as shown in drawing 9 (b).

[0049]Since a gate line is driven using the method of the 3rd and 4th examples of this invention, In drawing 3, the top frame memory 410 transmits image data to the top data actuator 210 at the same order as the recording order of image data, and the lower frame memory 420 transmits image data to the lower data actuator 220 at an order opposite to the recording order of image data. The upper gate actuator 310 and the lower gate actuator 320 output a gate ON signal one by one from the first gate line G1 of an upper gate line block, and the gate line G2m of the last of a lower gate line block, respectively. Drive methods other than

[in the 3rd and 4th examples] this are the same as that of what was mentioned above based on drawing 3.

[0050]When driving a liquid crystal display according to the 3rd and 4th examples of this invention, the pixel of two pixel rows in an interface is influenced in the same direction with the voltage impressed to the data line. Therefore, since the difference of the quantity of the light which penetrates the liquid crystal material in the pixel of a boundary part is small, the luminosity of a boundary part almost becomes homogeneity. As a result, the striped pattern generated in the boundary part of the conventional upper panel and a bottom panel does not appear.

[0051]According to this invention, like the above explanation, luminosity heterogeneous phenomena can be prevented by carrying out the scanning direction of the gate line of an upper panel in the direction opposite to the scanning direction of the gate line of a lower panel. Although this invention is explained based on the above most practical and desirable example, it is not limited to such an example and all of the structure of the equivalence contained in a generic claim and thought and various modification are included.

[Translation done.]

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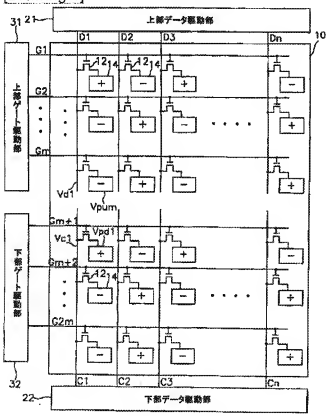
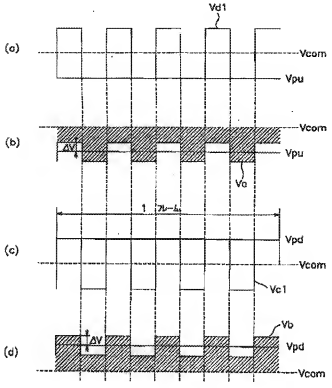
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

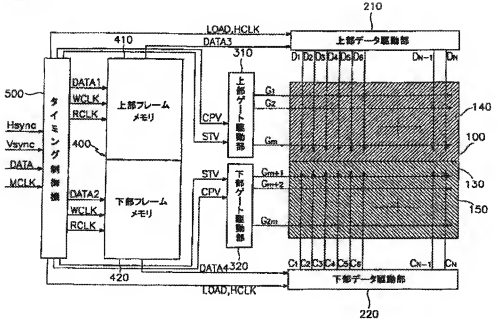
[Drawing 1]



[Drawing 2]

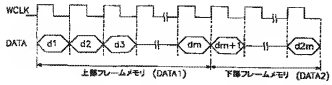


[Drawing 3]

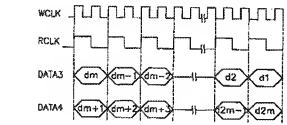


[Drawing 4]

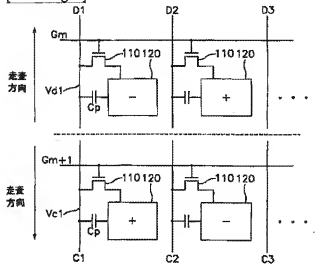
(a)



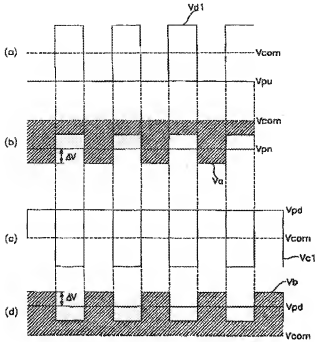
(b)



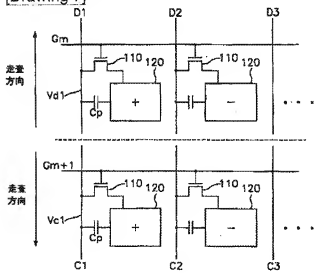
[Drawing 5]



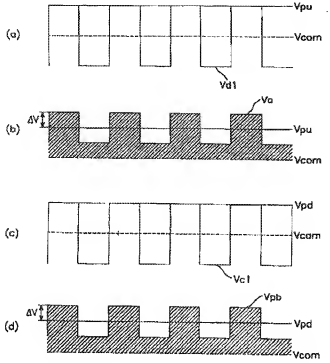
[Drawing 6]



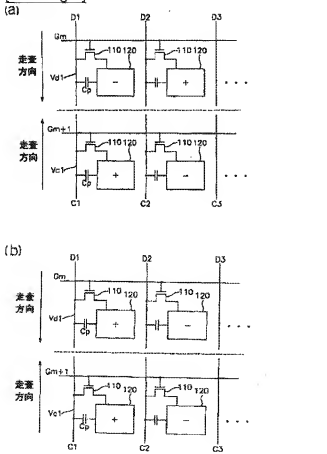
[Drawing 7]



[Drawing 8]


(a)
Vpu
Vcom
Vd1
(b)
ΔV
Va
Vpu
Vcom
(c)
Vpd
Vcom
Vc1
(d)
ΔV
Vpb
Vpd
Vcom

[Drawing 9]


(a)
D1
D2
D3
Gm
走査方向
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120
Vd1
Cp
Gm+1
Vc1
C1
C2
C3
(b)

[Translation done.]